

DDR3 Mini DIMM Slot Interposer

DDR3-1600 Mini DIMM Digital Validation

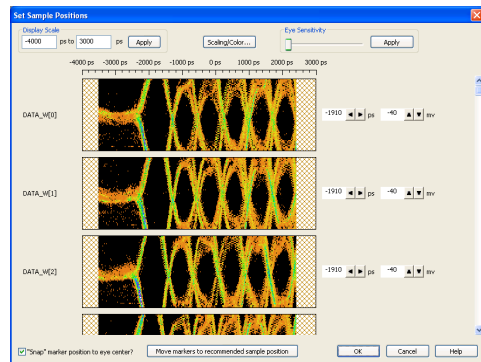
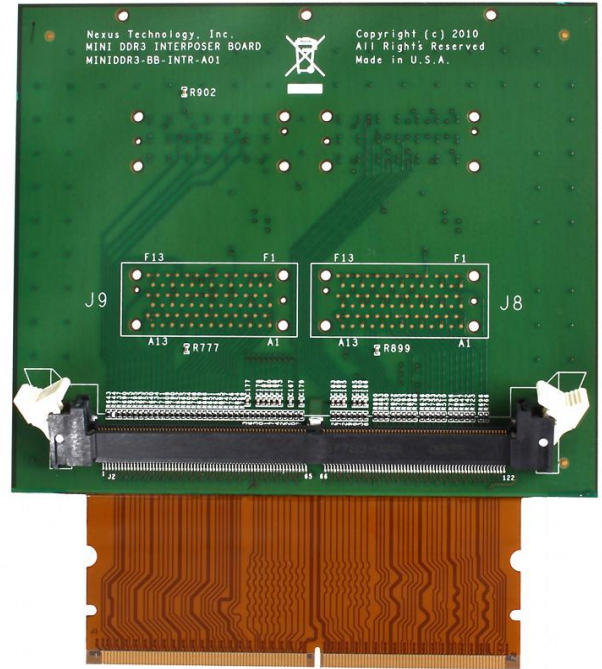
- High Speed DDR3 Digital Validation
- Passive 244-pin Mini DIMM Slot Interposer
- Compatible with Agilent Software Applications
- Acquisition up to DDR3-1600
- Supports JEDEC PC3-12800, PC3-10600, PC3-8500, and PC3-6400 DDR3 modules

Passive Interposer Design

This interposer is an extender design, does not require a dedicated Mini DIMM slot, and provides a quick & easy connection between your target DDR3 bus and an Agilent logic analyzer. This is a passive interposer with no added buffers to conceal system performance.

Software

This product comes with logic analyzer setup software, DDR3 protocol decode software and is fully compatible with Agilent's DDR3 Eye Finder software and Protocol Compliance & Analysis tool (B4622A).



DDR3 Eye Finder Software

The Agilent DDR3 Eye Finder software (freely available from Agilent) can be used to set valid read and write data eyes for proper state acquisition of DDR3 read and write data. This tool can also be used to analyze the analog characteristics of the read and write data eyes as seen by the logic analyzer. This information can be useful when debugging physical layer issues on the DDR3 data bits (DQ data channels).

Figure 1 Full-sensitivity Eye Finder results of this interposer.

DDR3 Command & Address EyeScan

The Agilent Logic Analyzers EyeScan tool (fully integrated with the Agilent Logic Analyzer application) can be used to quickly analyze the analog characteristics of the DDR3 command and address bus. With a horizontal resolution of 5ps, EyeScan can be used to identify problem signals quickly for further investigation with an oscilloscope. Results can be viewed for each individual signal or as a composite of multiple signals or buses.

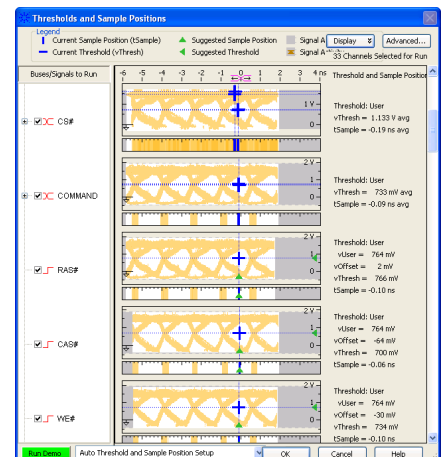


Figure 2 EyeScan results of this interposer.

DDR3 Protocol Compliance & Analysis

The Agilent DDR3 Protocol Compliance & Analysis tool (Agilent product B4622A, available for purchase separately) enables automated measurement of deep DDR3 bus traces to help identify protocol problem areas and give an overview of the system performance.

- Automates DDR3 protocol compliance
- Quickly identifies protocol violations and timing errors
- Allows user defined timing parameters
- Provides test results in HTML format
- Provides quick overview of DDR3 bus performance
- Enables fast trigger setup

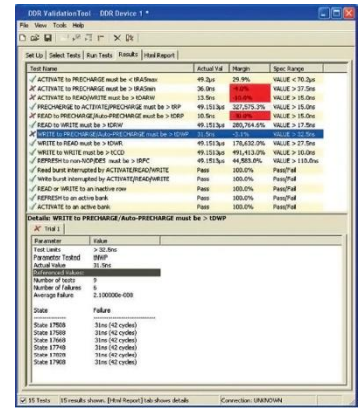


Figure 3 DDR3 Protocol Compliance & Analysis

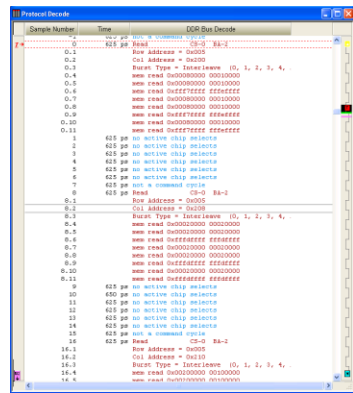


Figure 4 Bus Decode of this intersper.

DDR3 Protocol Decode

The NT-DDR3-DECODE memory bus decoder (included with this product) integrates with the Agilent Logic Analyzer software and sets up the logic analyzer and decodes the acquired data in a standard listing window. This allows for easy analysis of the DDR3 protocol, addressing, and read/write data from the DDR3 bus. This product also supports the Agilent memory bus decoder (B4621A, available for purchase from Agilent).

- Handles any read or write offsets (latencies)
- Burst lengths of 4, 8, or On-The-Fly
- Data Masking
- Read and Write data decoding

Command/Address Acquisition

This interposer provides excellent signal fidelity at speeds up to DDR-1600.

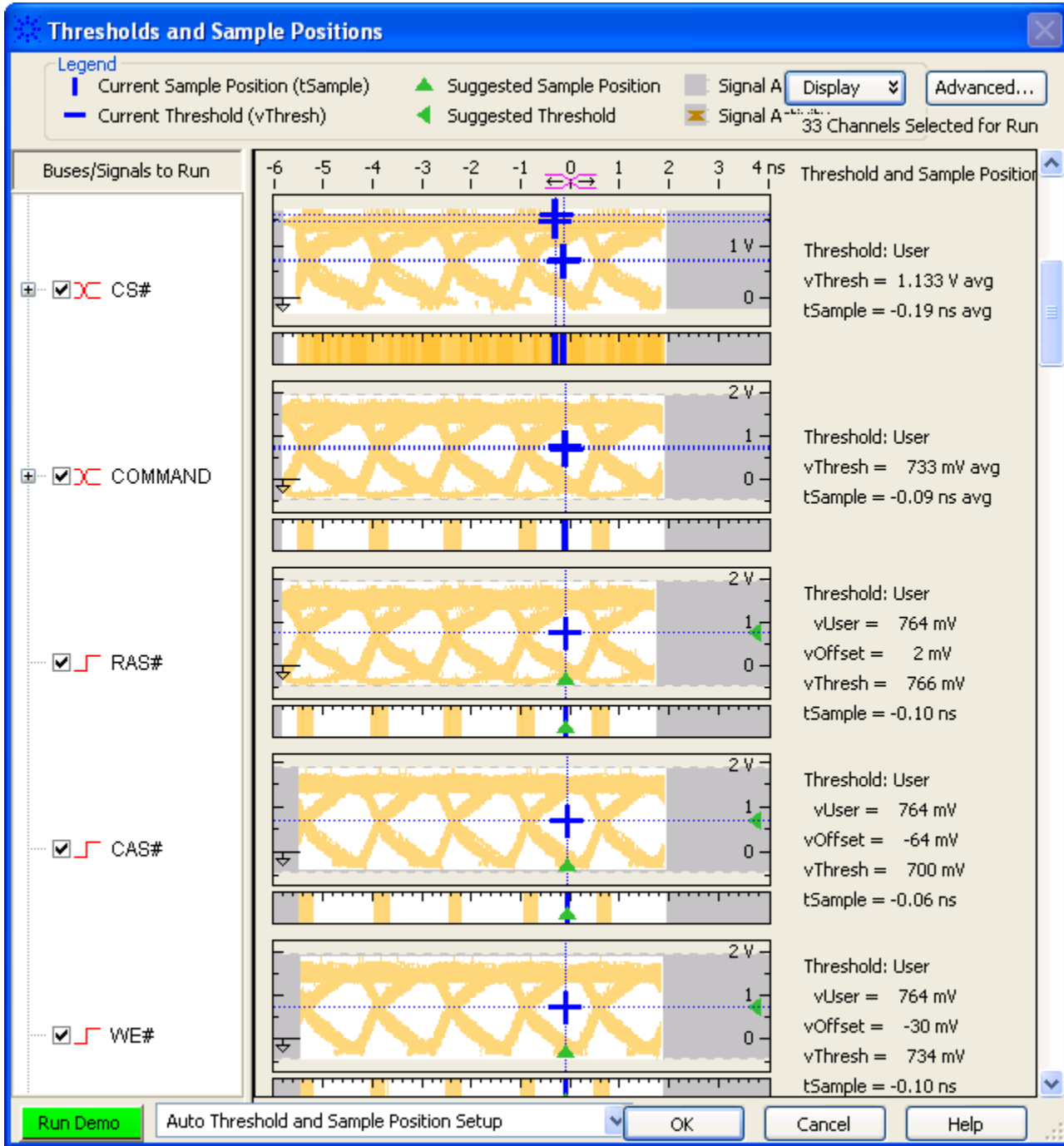


Figure 5 Eye Scan results of this interposer

Read & Write Data Eye Acquisition

This interposer also provides excellent signal fidelity for the read and write data as seen in the DDR3 Eye Finder figure below.

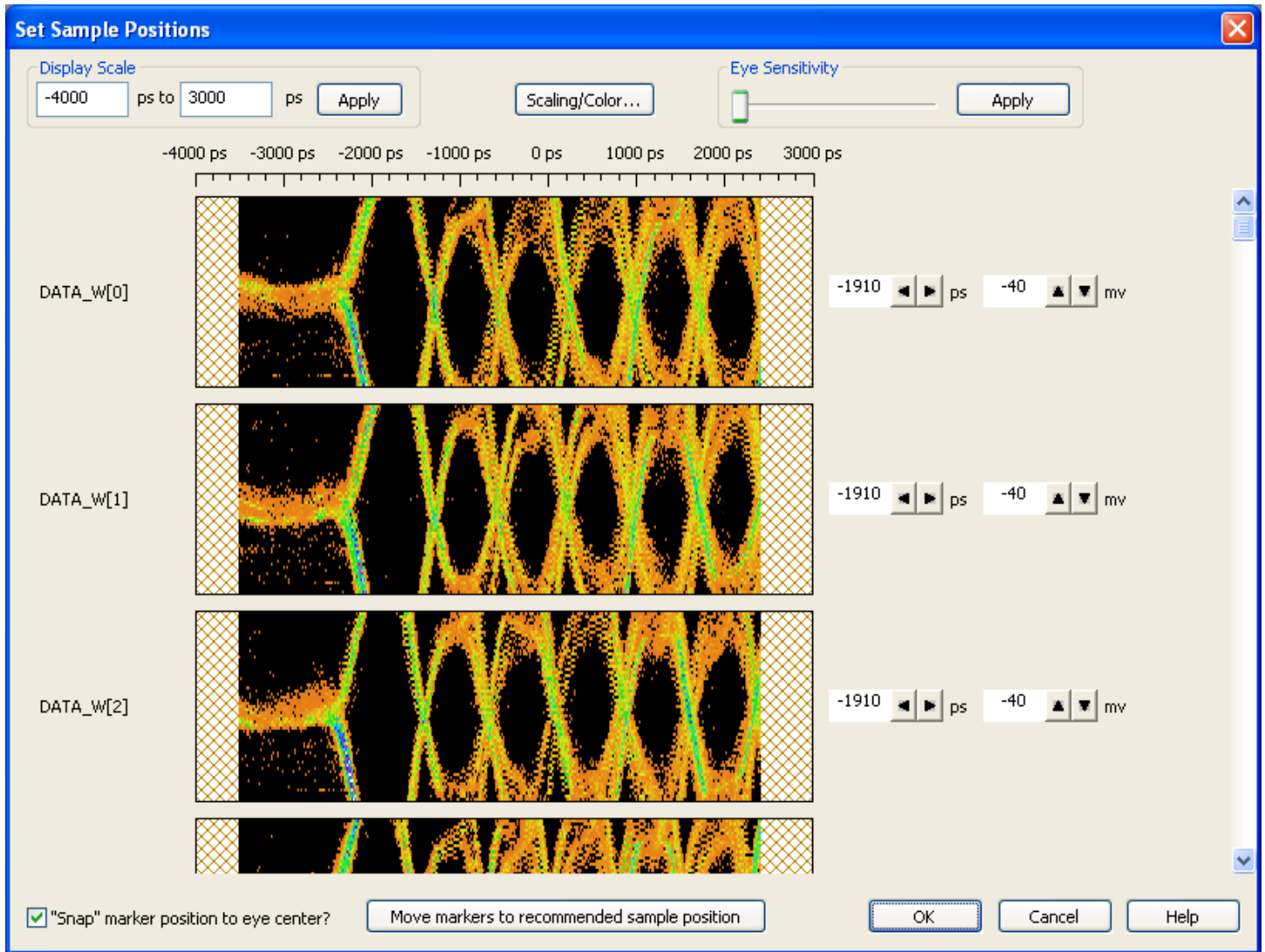


Figure 6 Full-sensitivity Write Data Eye Finder results of this interposer.

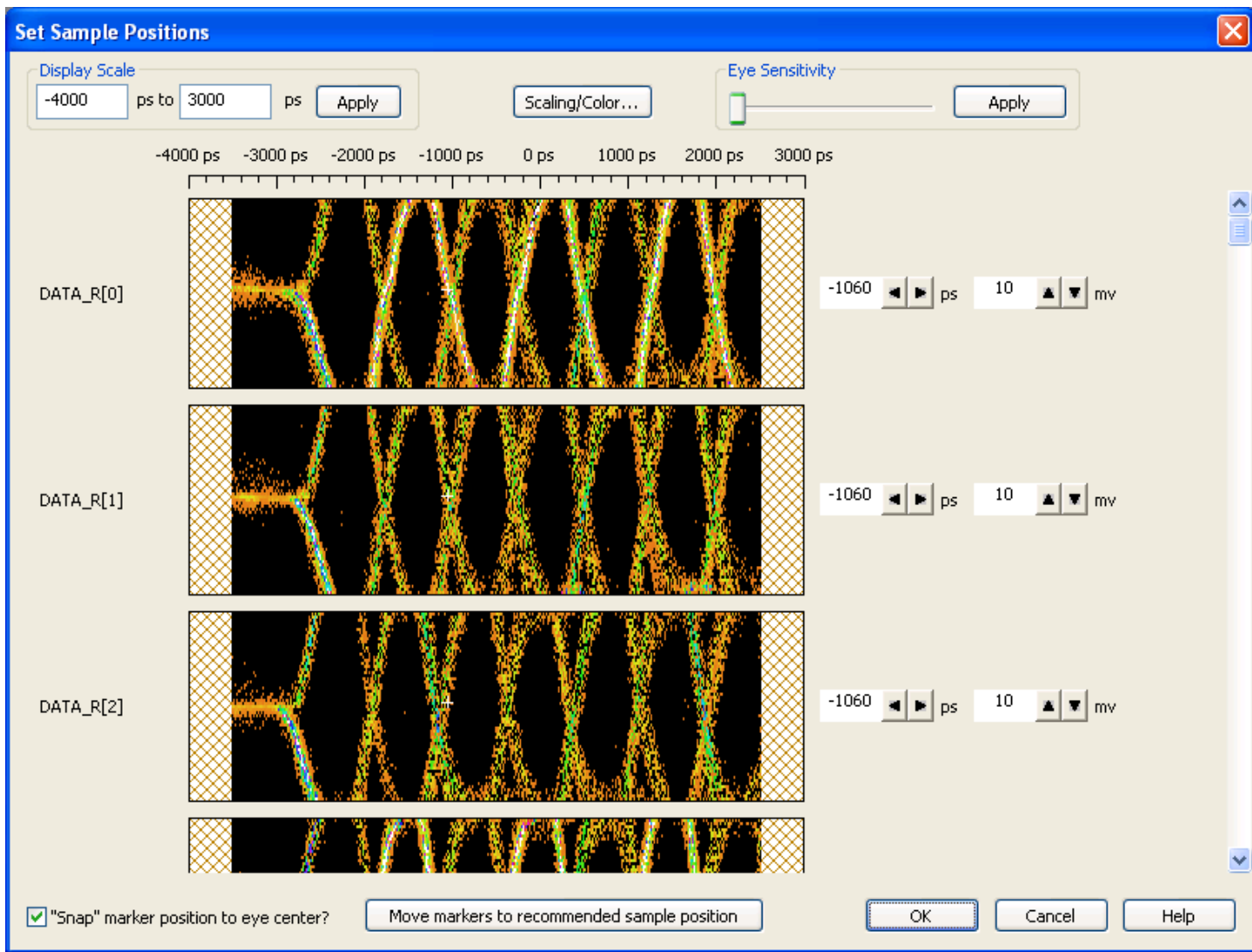


Figure 7 Full-sensitivity Read Data Eye Finder results of this interposer.

Bus Decode

The high fidelity of the signals, as seen in the previous sections, allows for very accurate state acquisition. This accuracy is critical for digital validation of DDR3, minimizing the time spent validating the connection and setup, and maximizing the time spent validating the target DDR3 bus.

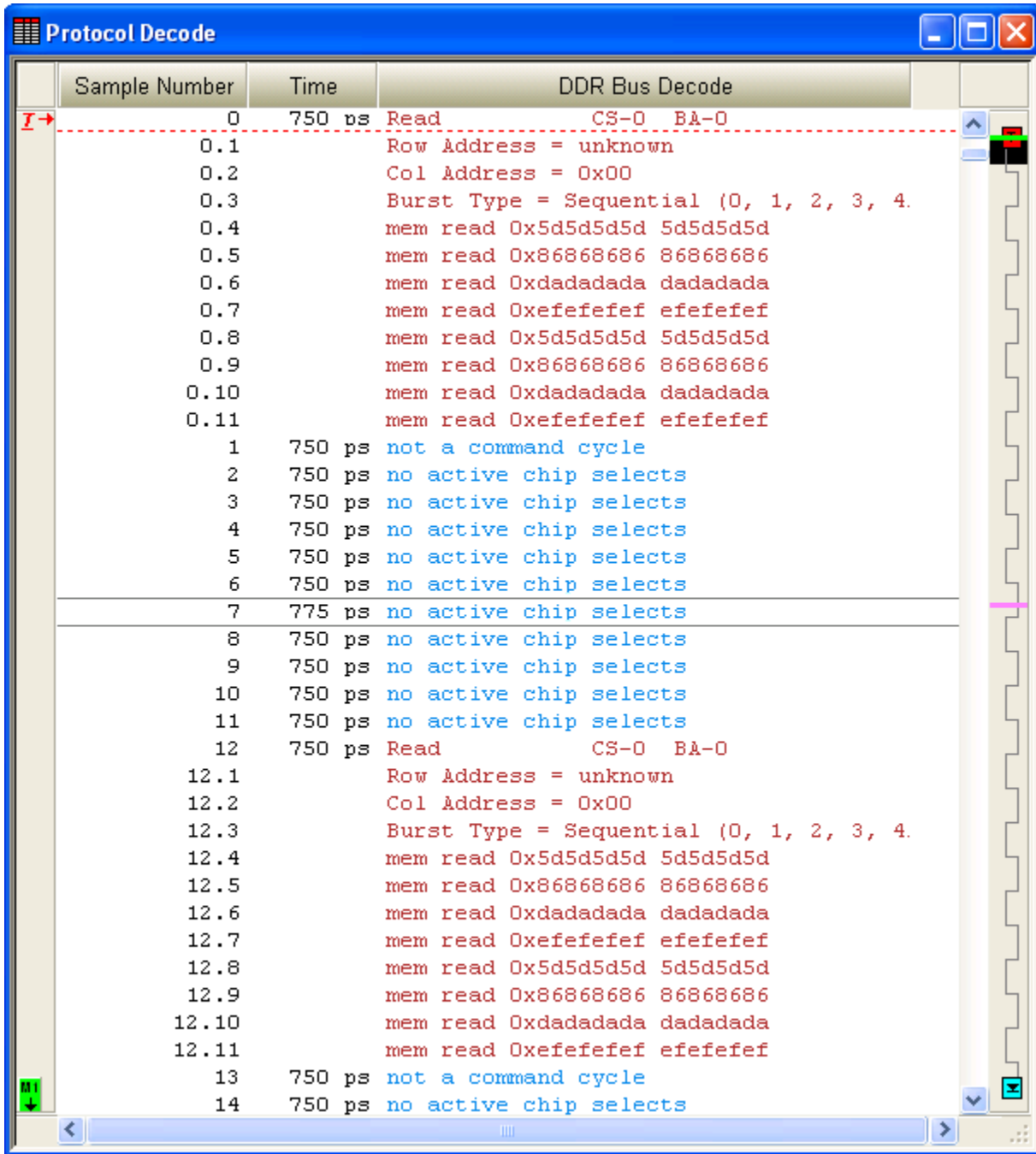


Figure 8 Bus Decode of this interposer.

DDR3 Mini DIMM Slot Interposer

NT-DDR3MDI Technical Specification

General

| Specification | Detail |
|--|--|
| Interface Type | Passive Interposer |
| LA Interface | Passive leash to Agilent modules. |
| JEDEC Module Type | DDR3 SDRAM Unbuffered Mini DIMM or DDR3 SDRAM Registered Mini DIMM |
| JEDEC Modules Supported | PC3-12800, PC3-10600, PC3-8500, PC3-6400 |
| Unbuffered DDR3 Data Rates Supported (MT/s) | 1600, 1333, 1067, 800 |
| Registered DDR3 Data Rates Supported (MT/s) ¹ | 1333, 1067, 800 |
| Min. Clock Edge-to-Edge | 500ps |
| Min. Voltage Swing | 200mV |
| Min. Eye Width | 200ps |

Agilent Hardware

| Specification | Detail | Quantity |
|--------------------------|--------------|----------------|
| Logic Analyzer Mainframe | 16902B | 1 |
| Logic Analyzer Module(s) | 16962A | 4 ² |
| Logic Analyzer Probes | None needed. | |

Supported Software

| Specification | Detail | Supported |
|----------------------------|--|------------------|
| Agilent Logic Analyzer S/W | 03.82.1024 or newer | Yes |
| Agilent DDR3 Eye Finder | | Yes |
| Agilent B4622A | Agilent Protocol Compliance & Analysis | Yes ³ |
| Agilent B4621A | Agilent Memory Bus Decoder | Yes ³ |
| Nexus NT-DDR3-DECODE | Nexus Memory Bus Decoder | Yes |

DDR3 Signals Probed

| Specification | Detail |
|-------------------------------|---|
| Command | RAS#, CAS#, WE#, CKE0, CKE1, RESET#, ODT0, ODT1 |
| Addressing | CS0#, CS1#, CS2#, CS3#, A00-A15, BA0-BA2 |
| Data Strokes | DQS0-DQS7 |
| Data Bits | DQ00-DQ63 |
| Data Masks | DM0-DM7 |
| ECC ⁴ (Check Bits) | CB0-CB7 |

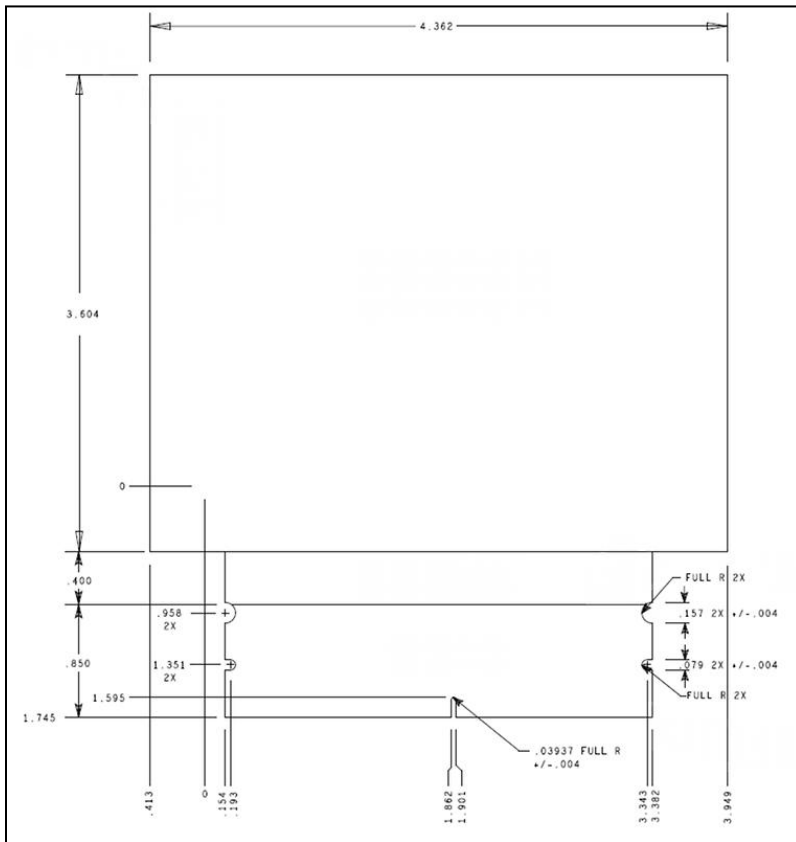
Product Configurations

| Nomenclature | Detail |
|------------------|--|
| NT-DDR3MDI(-LSH) | 1- DDR3-1600 Mini DIMM Slot Interposer 1- NT-DDR3-DECODE DDR3 Memory Bus Decoder SW License |

Notes

- 1: Please contact us for the most up to date information on registered DDR3 support at speeds above DDR3-1333.
- 2: Only one 16962A module is needed for DDR3 protocol analysis (DDR3 command & address acquisition). Four modules are needed for DDR3 command, address, read, and write data acquisition.
- 3: This product is fully supported and is available for purchase separately from Agilent.
- 4: Acquisition of ECC channels does **not** change the hardware requirements. Only four Agilent 16962A modules are required for full DDR channel acquisition which includes all command, address, strobes, data, masks, and ECC channel acquisition.

Product Mechanical Outline



Further Information

Please contact us by telephone, email or mail as listed below. Normal business hours are 9:00 – 5:00 EST.

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